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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LIN, JAMES	

ART UNIT	PAPER NUMBER
1762	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,139	CHANG, JUNG-CHIEN	
	Examiner	Art Unit	
	Jimmy Lin	1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-8 and 17-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami et al. (U.S. Publication 2003/0160339) in view of Kurita et al. (U.S. Patent 6,399,891).

Ikegami teaches a method of making an electronic component (abstract), wherein a first circuit layer 7 is formed on a substrate 15. An electronic element 9 is electrically connected to the first circuit layer, an encapsulant layer 11 is applied, and the substrate is removed ([0031], [0037] – [0038]; Figs. 2A – 8).

Ikegami does not explicitly teach depositing a resin-copper coating on the first circuit layer, forming a second circuit layer to serve as the topmost circuit layer, and connecting electronic components to the topmost circuit layer. However, Ikegami does teach connecting an electronic element connected to the first circuit layer. Kurita teaches a method of making an electronic element that has connecting parts that are subjected to low thermal stress and is free from breakage at connecting parts (cols. 1-3), wherein the electronic element comprises a resin layer 12, a copper layer 21, and a topmost circuit layer 26 (abstract; Fig. 1). Electronic

components 110, such as transistors, can be connected to the topmost circuit layer (col. 1, lines 13-19; Fig. 3b). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have electrically connected the electronic element of Kurita onto the first circuit layer of Ikegami so as to take advantage of an electronic element having low thermal stress at the connecting parts.

Kurita does not teach connecting multiple transistors onto the topmost circuit layer. However, transistors control the flow of current in electronic equipment. One skilled in the art would use multiple transistors in order to better and more precisely control the flow of current. Therefore, connecting multiple transistors to the topmost circuit layer would have been an obvious modification.

Ikegami and Kurita do not explicitly teach that the substrate is removed after the step of connecting the electronic components to the topmost circuit layer. However, Ikegami does teach that the encapsulant layer is applied before removing the substrate. Therefore, the electronic component of Kurita must necessarily be connected to the topmost circuit layer before applying the encapsulant layer and removing the substrate.

Claim 2: Ikegami teaches that the substrate has a plurality of fine holes and electrically conductive protrusions are formed on portions of the conductive film ([0013], [0033]; Fig. 4). By definition, a hole can be an indentation or depression. A dimple is also defined as a slight indentation or depression in a surface.

Claim 3: Ikegami teaches that the substrate has a flat surface between the holes (Fig. 4).

Claim 4: Kurita teaches that holes are formed in the resin layers and between the conductive layers and filled with electrically conductive material by plating or other means to electrically connect the various layers (column 5, lines 43 – 51).

Claims 5-8: Ikegami teaches that bonding wires are suitable to electrically connect two components (paragraph 31, lines 17 – 20).

Claim 17: Kurita teaches that a second circuit layer 22 and a third circuit layer 23 can be deposited before forming the topmost circuit layer 26 (Fig. 1).

4. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami '339 in view of Kurita '891 as applied to claims 1-4 above, and further in view Farnworth (US 6,365,501).

Ikegami and Kurita are discussed above. Kurita teaches that the electronic component can be connected with solder balls 112 (col. 1, lines 13-19), but does not teach that the solder balls are made of tin. However, Farnworth teaches that solder balls are generally formed of lead and tin and are used to join a chip to a carrier such as printed wiring board (column 3, lines 5 – 21). The selection of something based on its known suitability for its intended use has been held to support a prima facie case of obviousness. Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have used tin solder balls as the particular solder material with a reasonable expectation of success because Farnworth teaches that such materials are suitable for making solder balls.

5. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami '339 in view of Kurita '891 as applied to claims 1-4 above, and further in view of Lin et al. (US 5,200,362), Carey et al. (US 5,672,260), and Meyrat et al. (US 4,842, 536).

Ikegami and Kurita are discussed above. Lin teaches a method of fabricating a semiconductor device, wherein the substrate is removed and isolating layers 23 can be applied to the exposed surface of the pattern of conductive traces 13 (column 3, line 66 – column 4, line 1; Fig. 6). Openings 24 are formed through the isolating films to expose selected portions of the pattern of conductive traces (column 4, lines 3 – 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have applied an isolating layer to the exposed first circuit layer of Ikegami. One would have been motivated to do so in order to expose only selected portions of the traces and to protect the non-selected portions.

Ikegami, Kurita, and Lin do not explicitly teach applying tin paste to the first circuit layer between adjacent isolating layers. However, Ikegami does teach that the exposed first circuit layer can be surface-mounted on an external printed wiring substrate through electrically conductive adhesive. Meyrat teaches that a tin paste soldering material can be arranged on a

circuit board, wherein surface mounted devices are then connected with the tin. Printed circuits manufactured this way can accommodate more components per unit surface area (col. 1, lines 12-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to apply tin paste to the selected portions of the exposed pattern of conductive traces of Lin. One would have been motivated to do so with the expectation of connecting the conductive traces to surface mounted devices in a space efficient manner.

6. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami '339 in view of Kurita '891 as applied to claims 1-4 above, and further in view of Whetsel (U.S. Publication 2002/0021140).

Ikegami and Kurita are discussed above. Kurita teaches that a transistor can be attached to the topmost circuit layer (col. 1, lines 13-19), but does not explicitly teach that the transistor can be embedded in the topmost circuit layer. However, Whetsel teaches that smaller transistors may be embedded within integrated circuits to enable the development of smaller, lower power electronic consumer products [0003]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have embedded a small transistor into the topmost circuit layer of Kurita. One would have been motivated to do so in order to make an integrated circuit capable of being used in small electronic consumer products.

Response to Arguments

7. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Lin whose telephone number is 571-272-8902. The examiner can normally be reached on Monday thru Thursday 8 - 5:30 and Friday 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JL
JL

BRET CHEN
PRIMARY EXAMINER